REMARKS

Claims 1-20 are pending in this application.

Claims 1-4, 6-10, and 12-20 have been rejected

Claims 5 and 11 have been objected to.

Claims 1-20 remain pending in this application.

Reconsideration and full allowance of Claims 1-20 are respectfully requested.

REJECTION UNDER 35 U.S.C. § 102

The Office Action rejects Claims 1-4, 6-10, and 12-20 under 35 U.S.C. § 102(b) as being unpatentable over U.S. Patent No. 5,574,633 to Prater ("Prater"). The Applicants respectfully traverse this rejection.

Claims 1, 7, and 13 recite that a "load portion" of a signal line is isolated from a "source portion" of the signal line. Claims 1, 7, and 13 also recite that the "load portion" of the signal line is connected to an "intermediate floating virtual source/sink."

These limitations, and their particular connections, are not taught or suggested by the art of record. The arguments and discussion of previous responses are hereby incorporated by reference and re-urged, with appropriate recognition of the amended claim terms.

The current Office Action appears to allege that the claim elements are reflected in Prater as follows:

- That the claimed signal line corresponds to a combination of Prater's next state input 40 as the source portion and lines n12 (hereafter, for clarity, only line 312 and other 3xx elements will be referenced) as the load portion;

- That the claimed floating virtual source/sink corresponds to Prater's charge sharing line 36; and
- That the charge redistribution circuit corresponds to a combination of Prater's 330, 314, and all of Prater's Fig 3.

If the undersigned has misunderstood or misinterpreted the Examiner's position, correction or clarification is invited.

The Examiner also alleges, with regard to the claim limitation "that connects it [the load portion] to the intermediate floating virtual source/sink during an idle period prior to a change of state", that "Component 48 generates the recited idle period." It does not appear that component 48 generates any idle period. Prater describes that "the state of each I/O pad 13 must be held in a register 48 to compare at 50 with the next state 40 of the I/O pad", which appears to be simple register storage of a current pad state, not a generation of any idle period.

Further, Prater describes that prior to a high-to-low transition, "transistor n25 of the respective pad driver n14 will be inactive, and transistor n27 of the respective pad driver n14 will be active. Signal n12 and I/O pad n13 will thus be driven to a logical ZERO during phase 3." (col. 9, lines 46-40). As such, signal 312 is driven to ground instead of connected to charge sharing circuit 36.

As such, Prater is seen not to anticipate independent claim 1 or independent claims 7 and 13, which contain similar limitations. As these distinctions apply to the respective dependent claims as well, all rejections are traversed.

With regard to claims 2, 4, and 6, the Office Action states that "Line 36 is seen as a charge storage element, a capacitor, or a floating conductor." Of course, while stating that

something "is seen" is a convenient conclusory statement, it does not meet the legal standard of an anticipation rejection. Prater does not appear to teach or suggest that charge sharing line 36 is seen as a charge storage element, a capacitor, or a floating conductor, as claimed. The Examiner is cordially requested to identify any such teaching in Prater. Similar limitations are found in claims 8, 10, 12, 14, 16, and 19.

For these reasons, Prater fails to anticipate the Applicants' invention as recited in Claims 1, 7, and 13 (and their dependent claims). Accordingly, the Applicants respectfully request withdrawal of the § 102 rejections and full allowance of Claims 1-4, 6-10, and 12-20.

Claims 5 and 11 were objected to as being dependent upon a rejected base claim, but were said to be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. In view of the Applicants' remarks set forth above, the Applicants respectfully submit that Claims 5 and 11 are also allowable without being rewritten.

The different structure of the presently claimed embodiments present a significantly different operation than does Prater. Prater deals with the charge sharing in simultaneous switching lines. According to Applicant's analysis, when at time t=T1 transitioning output are shorted for a certain amount of time, energy is recycled and high to low-going output supplies charge to low to high-going line. This reduces amount of power consumption and at the same time results in reduction in ground bounce.

In Prater, then, the advantage of power reduction is statistical in nature and depends on direction of switching. By Applicant's analysis, the best case scenario is when half of the switching lines are going from one to zero and half of the switching lines are going from zero to one. This is described in Prater, for example, at col. 5, lines 5-65.

Prater also connects the switching signal lines to line 36. This line has a very small

capacitance, if any, as compared to load portion capacitance. Thus, any advantage of power reduction is statistical in nature and at any particular time depends on the number of lines switching in one direction at that time as described in col. 5, lines 20-60. Since this line has at best a very small capacitance, the steady-state potential is independent of potential of the line, as is clearly expressed in the equations presented in Prater's col. 5.

Prater further described its timing events with reference to Figure 4. Prater also gives a method of generating a control signal for the required operation, as illustrated in Figure 3, where the previous state is stored in a register and at the time of system clock it is compared with next state to determine transitioning output.

In contrast, various embodiments of the present application provide a chip level intermediate floating virtual source/sink..This system can provide a steady-state, statistically-independent power reduction advantage.

As can be seen in the specification as filed, the virtual floating source/sink has a very large capacitance as compared to a switching line, and thereby provides statistically-independent power savings. For example, the power savings are not dependent on number of simultaneous switching lines. Different lines switching at different times source or sink charge to the floating source/sink or mesh.

In various embodiments of the present invention, whenever a line is having a transition for a defined time, it is connected to virtual source/sink which, depending on the direction of transition this virtual source/sink, gives charge or takes charge from the transitioning line. Since this floating mesh acts a charge reservoir, it is not necessary that all the transitioning lines should be connected simultaneously. Further, the intermediate level speeds up the rate of charge transfer since it has to travel from capacitor to the circuit rather than from one circuit to another.

Shorting by a single net is not equivalent to chip level mesh generation.

Since the techniques described in the instant application are based on a virtual floating source/sink approach it is not necessary that transitions should be at the same time. This enables use of independent transition detection pulse generator circuitry. Here each line is delayed and compared so as to detect any transition, which can accommodate the common case where different lines in a chip can be switching at different interval. A virtual mesh also provides reduction in power consumption even when only single line is switching.

Accordingly, the Applicants respectfully request the allowance of Claims 1-20.

CONCLUSION

The Applicants respectfully assert that all pending claims in this application are in condition for allowance and respectfully request full allowance of the claims.

SUMMARY

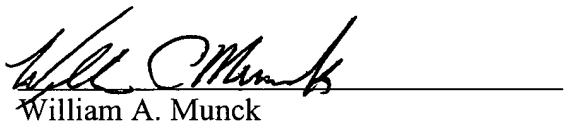
If any outstanding issues remain, or if the Examiner has any further suggestions for expediting allowance of this application, the Applicants respectfully invite the Examiner to contact the undersigned at the telephone number indicated below or at *wmunck@davismunck.com*.

The Commissioner is hereby authorized to charge any fees connected with this communication (including any extension of time fees) or credit any overpayment to Deposit Account No. 50-0208.

Respectfully submitted,

DAVIS MUNCK, P.C.

Date: Dec. 12, 2005



William A. Munck
Registration No. 39,308

P.O. Drawer 800889
Dallas, Texas 75380
Phone: (972) 628-3600
Fax: (972) 628-3616
E-mail: *wmunck@davismunck.com*